

New Challenges in Compliance Test and Debug for PCIe® 16GT/s

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Agenda

- **PCIe® Overview including what's new with PCIe 4.0**
- **PCIe Transmitter Testing**
- **PCIe Receiver Testing**
- **Intro to PCIe Tx and Rx Test Solutions**

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PCIe Compliance Testing

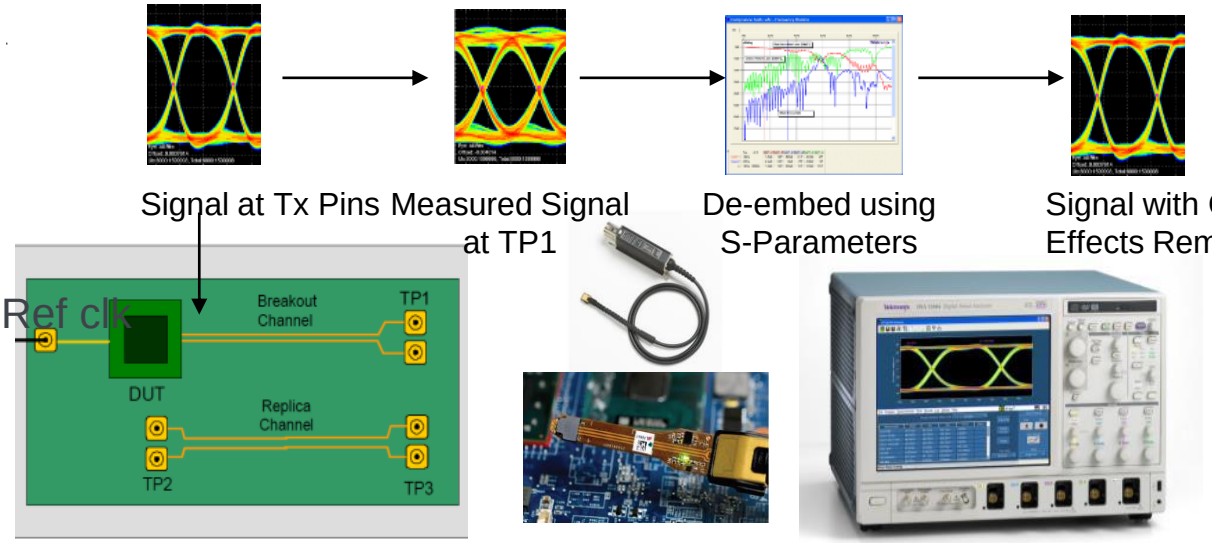
- **PCI-SIG holds regular compliance workshops/plugfests typically 4x/yr**
- **Vendors who desire to be on PCI-SIG Integrator's List attend PCI-SIG workshops where they must pass all four electrical tests & 80% of interoperability tests**

PCIe 3.0 Electrical PHY Compliance Tests
Transmitter Testing
Receiver Jitter Tolerance Testing
Tx/Rx Link Equalization Testing
PLL Loop Bandwidth Testing

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Base Spec Tx Testing

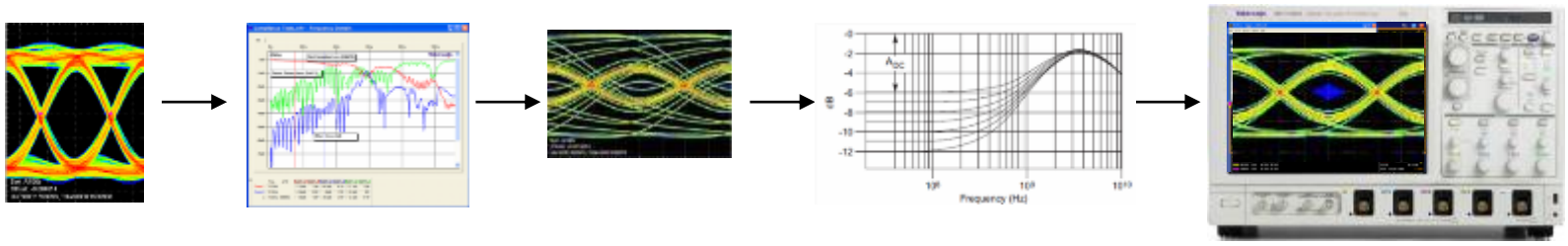
- **Base Specification Measurements are defined at the pins of the transmitter**
- **Signal access at the pins is often not possible**
- **De-embedding is required to see what the signal looks like at the pins of the Tx, without the added effects of the channel**
- **S-Parameters are acquired on the replica channel**
- **Measurement at Tx pins can also be enabled by high fidelity probes, eg P7700**



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CEM & U.2 Spec Tx Testing

- **CEM Specification Measurements are defined at the slicer of a receiver**
- **Signal access is not possible**
- **Embedding of the compliance channel and package, as well as application of the behavioral equalizer is required**
- **SigTest or custom software like DPOJET will perform the embedding and calculate measurements**



Signal Acquired from Compliance Board | **Embed Compliance Channel and Package** | **Closed Eye due to the Channel** | **Apply CTLE + DFE** | **Open Eye for Measurements**

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PCIe 4.0 Changes

- **16 GT/s, using scrambling, same as 8 GT/s, no encoding change**
- **Reduction in RJ (random jitter) from 3ps (PCIe 3.0) to ~1ps (PCIe 4.0) for stressed eye parameters *[PCIe Base Spec, Table 9-10]***
- **PCIe 4.0 connector enhanced electrically**
 - Connector now included in test fixtures for both Base and CEM
- **Behavioral Rx EQ data rate dependent**
- **Limited channel: ~12” for 1 connector (including 4” AIC); requires use of repeater (both redriver & retimer) for longer channels and/or 2nd connector**

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PCIe 4.0 Changes (continued)

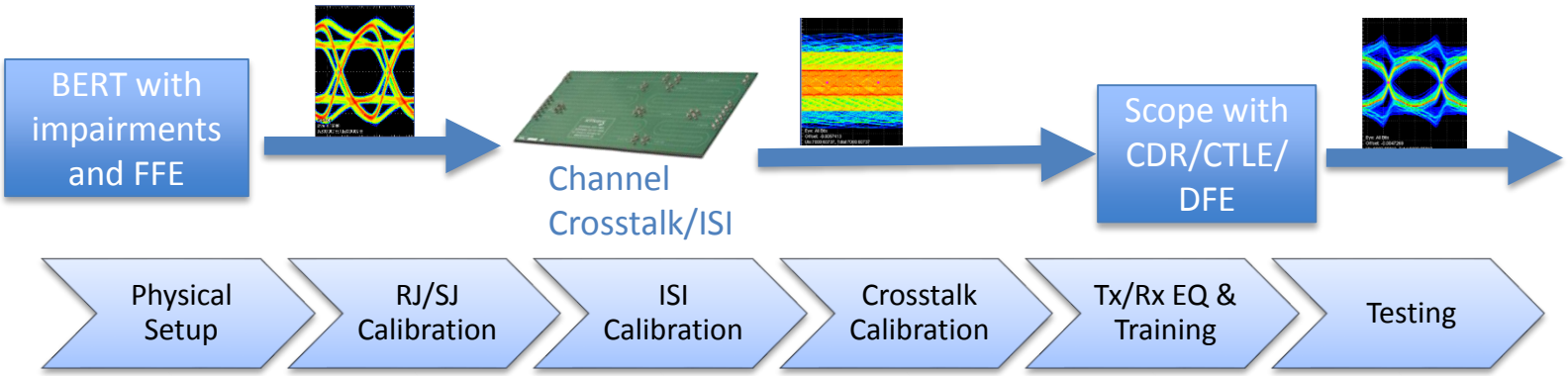
- **New 'SRIS' independent RefClk modes**
 - SRNS – Separate RefClk Independent with No SSC Architecture
 - SRIS – Separate RefClk Independent with SSC Architecture
- **New Rx Lane Margining feature measures EH/EW margin at end of channel**
- **Eye height for PCIe 4.0 reduced to 15mVpp**

Note: This presentation is based on the 0.7 draft PCIe 4.0 CEM specification and numbers, etc. are subject to change.

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Receiver Test Overview

- **Need fully integrated test system, including HW and SW solutions**
 - Reliably put device under test into loopback mode
 - Facilitate link equalization training to optimize the channel, including built-in TxEQ and RxEQ optimization
 - Calibrate and sweep full suite of impairments (ISI, RJ, DMSI, CMI)
 - Debug DUT-specific problems with BER, FEC, and link training
- **Solution must cover multiple speeds and spec generations (eg PCIe 3.0, PCIe 4.0, etc.)**



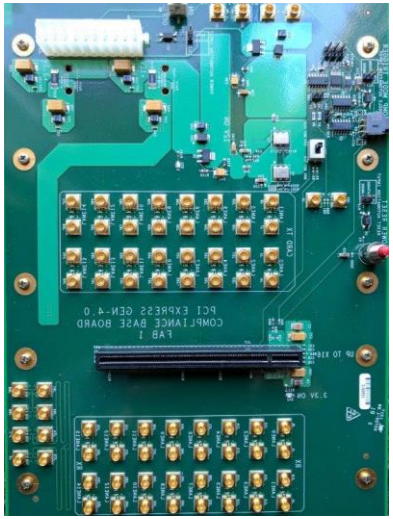
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Rx Test for PCIe 4.0

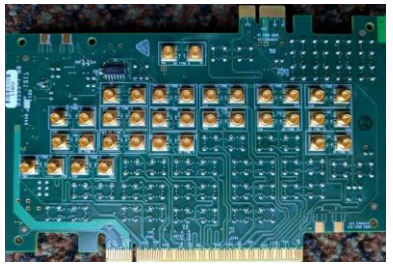
- **New fixtures for both BASE and CEM**
 - PCIe 4.0 adds concept of variable channel length to converge on correct eye opening
 - CEM fixtures:



CBB Variable ISI



CBB



CLB

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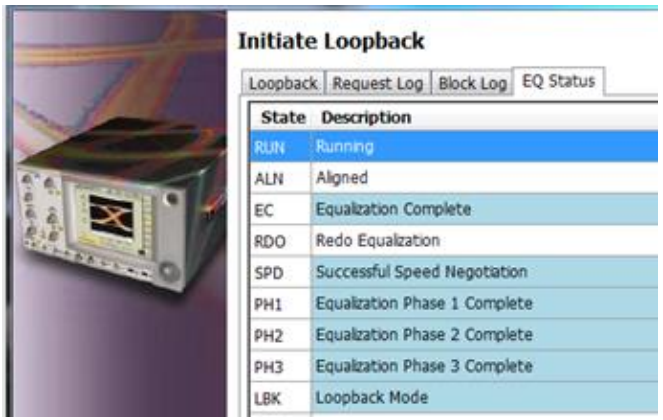
PCIe 4.0 CEM Rx Calibration

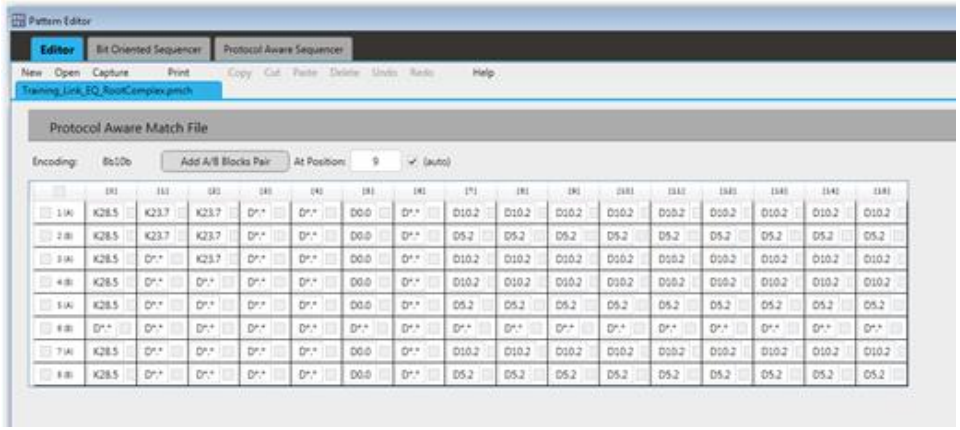
- **Calibrate Amplitude, Rj, Sj@100MHz (1m cable to oscilloscope)**
- **Establish 30dB, 28dB and 27dB channels**
 - Vary the CBB Variable ISI Pair
 - BERT➔1m SMA cable➔CBB Variable ISI brd➔300mm SMP cable➔CBB Rx Lane0➔CLB Tx Lane0➔300mmSMP cable➔CLB Variable ISI brd➔1m SMA cable➔Scope (embedding refpkg model)
- **Calibrate DMI (14mV) and CMI (150mV) @ end of channel**
- **Find Optimal Tx EQ Preset (27db channel)**
- **Increase channel loss from 27 - 30dB using the CBB Variable ISI board**
 - Find loss where EW/EH drop below targets and step back one pair
- **Ensure Preset is still optimal**
- **Vary the following until EW(18.75 +/-0.5)/EH (15mV +/-1.5) targets are met**
 - Sj (5-10ps)
 - DMI (10-25mV)
 - Amplitude (720-800mV)
 - Record Final Settings

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Debugging Handshaking Issues

- **Two phase link equalization**
 - Complete 8G link eq → begin 16G link eq
- **BERT displays LTSSM status and logs.**
- **Programmable BERT detector pattern matching allows creation of customized handshaking for debugging**





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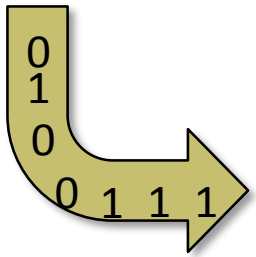
Debugging Handshaking Issues

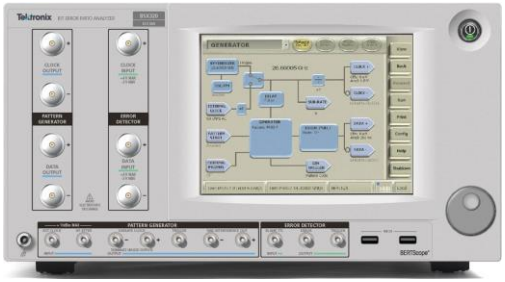
- **Link layer decoding**
- **Decodes and displays PCIe data using characters and names that are familiar from the standard, such as:**
 - SKP
 - Electrical Idle
 - EIEOS
- **Results table shows time-correlated listing of events time-correlated with waveform view**
- **Integrated search with marks**
- **Can be triggered using BERT detector protocol pattern matcher**

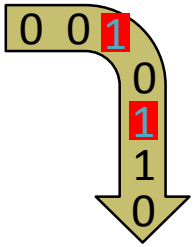


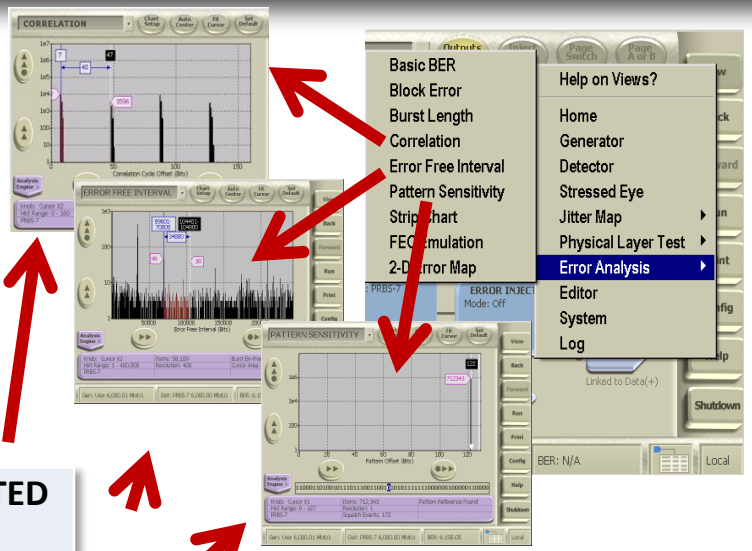
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Debugging Physical Layer Issues









BER = 3.9×10^{-9}

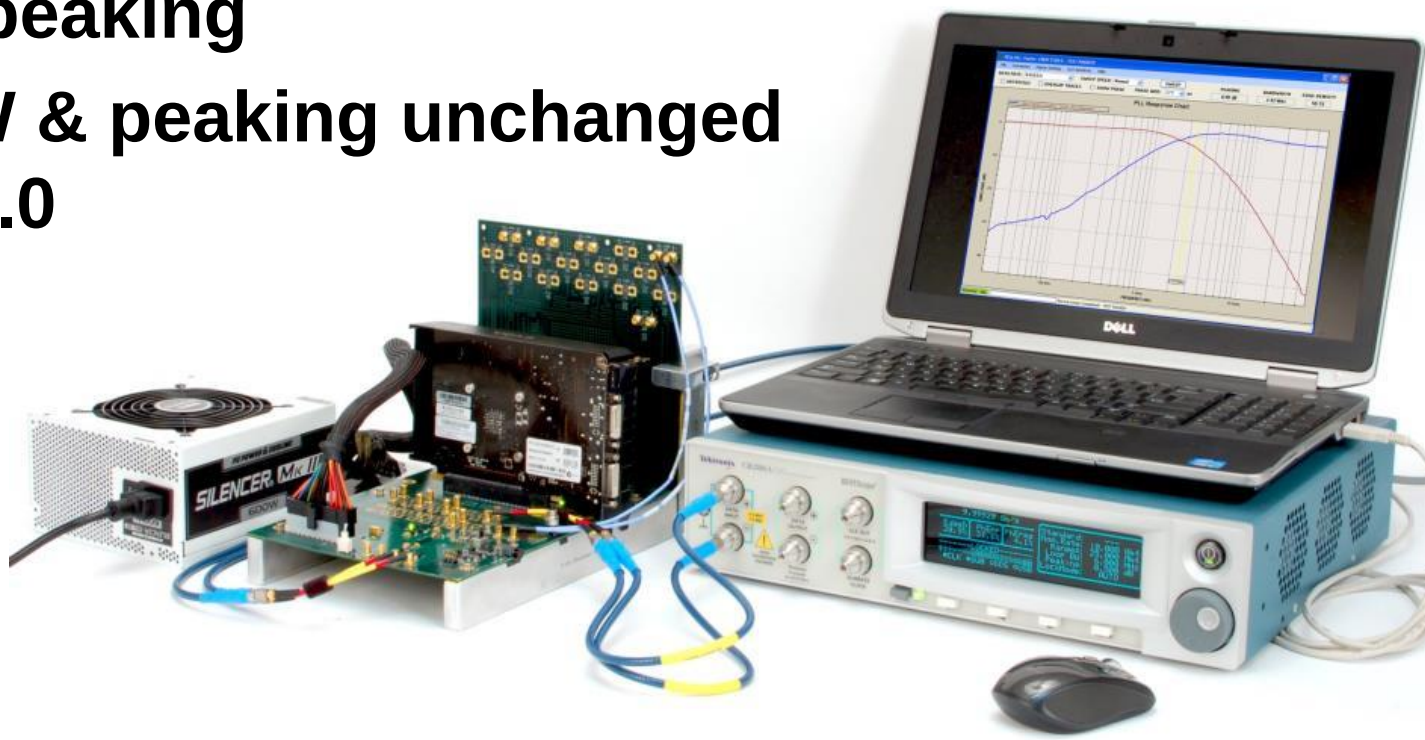
ERROR BIT LOCATION	EXPECTED BIT
200,457	0
1,247,356	1
1,447,890	0
3,885,245	0
4,001,876	1
8,233,191	0
…	

Knowing *error locations* points to *Error Patterns* which lead to unique debugging information. This allows you to “virtually probe” inside your DUT

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PLL Loop Bandwidth Test

- **Phase modulate of reference clock and measure phase error on DUT Tx**
- **Software on PC plots loop bandwidth/peaking**
- **PCIe 4.0 BW & peaking unchanged from PCIe 3.0**



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Tx/Rx Link Equalization Testing

- **Under automation, BERT issues EQ request to the DUT and simultaneously generates trigger signal for Scope.**
- **Scope measures time to complete EQ change on DUT output**



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Conclusion

- **PCIe 4.0 introduces new test calibration and test methodologies, including new fixtures**
- **Evaluation of Rx and Tx compliance solutions is now underway**
- **Handshaking for loopback and equalization training is now available**
- **Debugging tools for physical layer and handshaking issues have advanced with the latest generation of Rx and Tx test equipment**

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